Introduction to Digital Logic

EECS/CSE 31L

**Assignment 1: 4-Input Multiplexer**

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**1 Block Description**

This block is designed to take in 2 inputs in order to select between another 4 inputs

**2 Input/Output Port Description**

|  |  |  |  |
| --- | --- | --- | --- |
| Port name | Port size | Port Type | Description |
| Input0 | 1 | IN | Value of first input |
| Input1 | 1 | IN | Value of second input |
| Input2 | 1 | IN | Value of third input |
| Input3 | 1 | IN | Value of fourth input |
| Select0 | 1 | IN | Gets the first select operand |
| Select1 | 1 | IN | Gets the second select operand |
| output | 1 | OUT | The operation result |

**3 Design Schematics**

**Truth Table:**

|  |  |  |
| --- | --- | --- |
| Sel\_1 | Sel\_0 | F |
| 0 | 0 | In\_0 |
| 0 | 1 | In\_1 |
| 1 | 0 | In\_2 |
| 1 | 1 | In\_3 |

**Boolean Expression:**

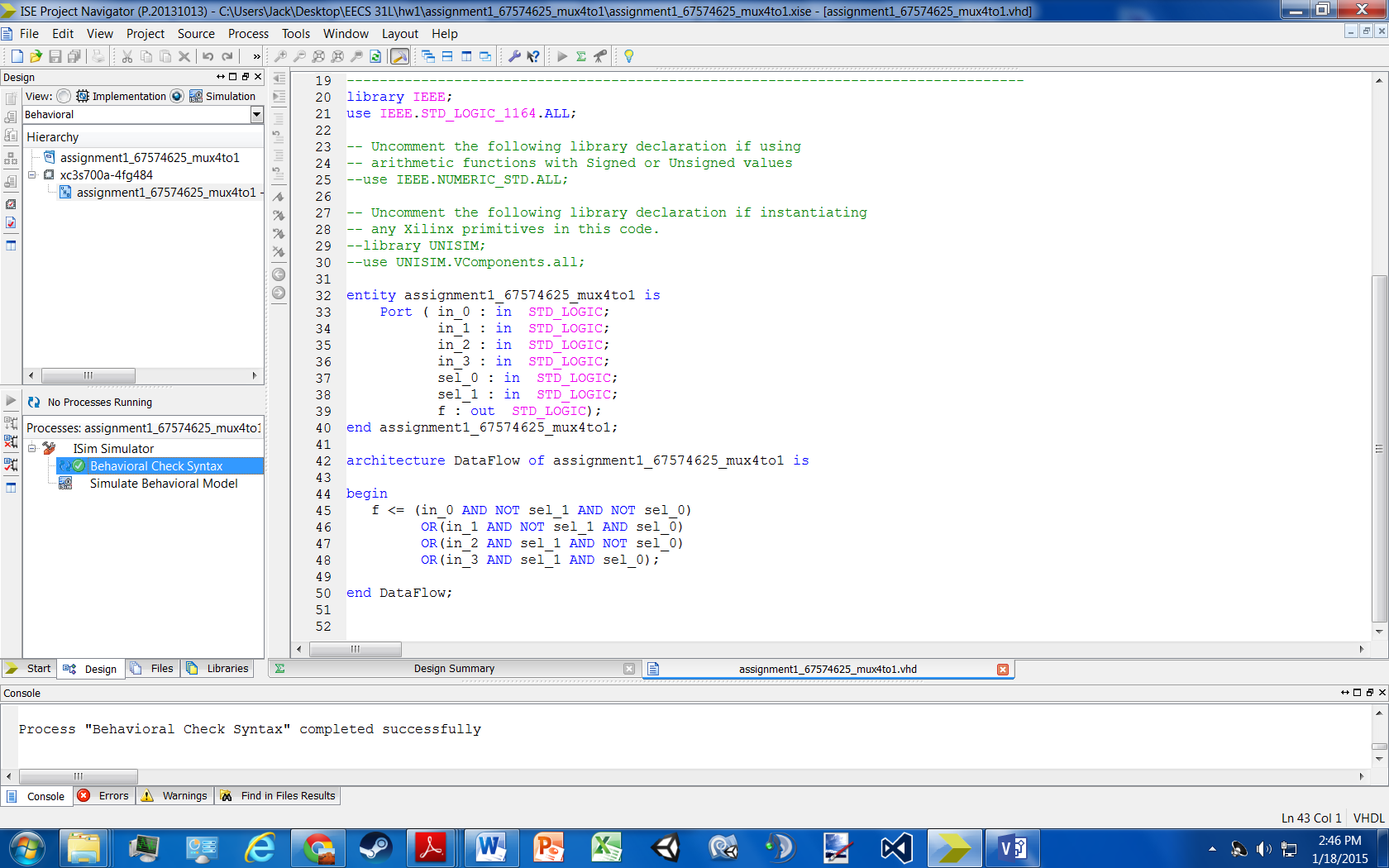
F = (Sel\_1’)(Sel\_0’)(In\_0) + (Sel\_1’)(Sel\_0)(In\_1) + (Sel\_1)(Sel\_0’)(In\_2) + (Sel\_1)(Sel\_0)(In\_3)

**Gate Representation:**

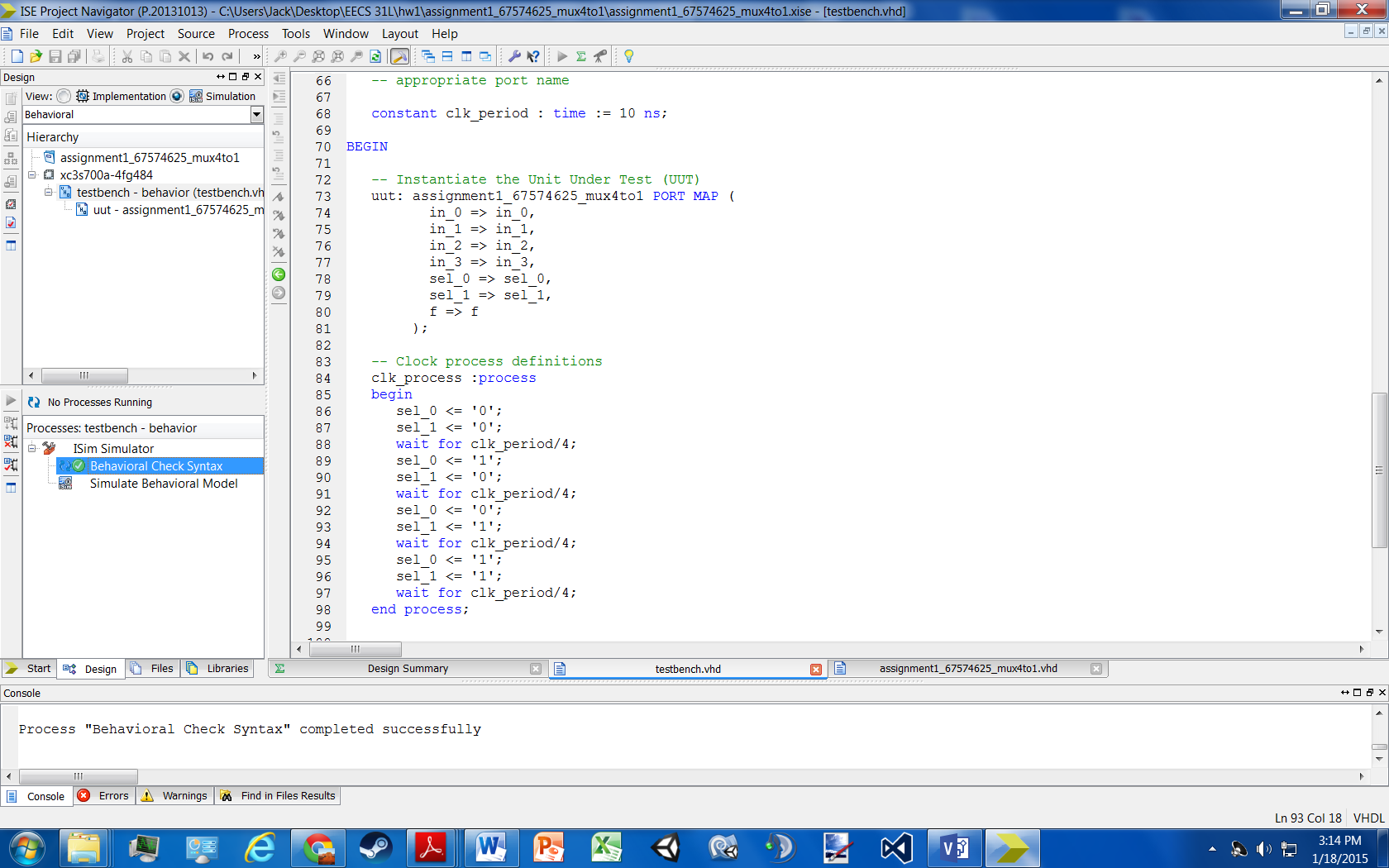


**4 Compilation**

4 to 1 mux code compiled



Testbench compiled



**5 Elaboration**

**Assumptions:**

* in\_0, in\_1, in\_2, in\_3 are only 1-bit
* f becomes ‘0’ when either in\_0 or in\_2 are selected because in\_0 and in\_2 = ‘0’
* f becomes ‘1’ when either in\_1 or in\_3 are selected because in\_1 and in\_3 = ‘1’
* Truth table above shows selection method.

**Errors:**

* No errors occurred while coding

**Simulation Log:**

Started : "Simulate Behavioral Model".

Determining files marked for global include in the design...

Running fuse...

Command Line: fuse -intstyle ise -incremental -o {C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1\_67574625\_mux4to1/testbench\_isim\_beh.exe} -prj {C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1\_67574625\_mux4to1/testbench\_beh.prj} work.testbench {}

Running: C:\Xilinx\14.7\ISE\_DS\ISE\bin\nt64\unwrapped\fuse.exe -intstyle ise -incremental -o C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1\_67574625\_mux4to1/testbench\_isim\_beh.exe -prj C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1\_67574625\_mux4to1/testbench\_beh.prj work.testbench

ISim P.20131013 (signature 0x7708f090)

Number of CPUs detected in this system: 4

Turning on mult-threading, number of parallel sub-compilation jobs: 8

Determining compilation order of HDL files

Parsing VHDL file "C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1\_67574625\_mux4to1/assignment1\_67574625\_mux4to1.vhd" into library work

Parsing VHDL file "C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1\_67574625\_mux4to1/testbench.vhd" into library work

Starting static elaboration

Completed static elaboration

Compiling package standard

Compiling package std\_logic\_1164

Compiling architecture dataflow of entity assignment1\_67574625\_mux4to1 [assignment1\_67574625\_mux4to1\_def...]

Compiling architecture behavior of entity testbench

Time Resolution for simulation is 1ps.

Waiting for 1 sub-compilation(s) to finish...

Compiled 5 VHDL Units

Built simulation executable C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1\_67574625\_mux4to1/testbench\_isim\_beh.exe

Fuse Memory Usage: 29848 KB

Fuse CPU Usage: 420 ms

Launching ISim simulation engine GUI...

"C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1\_67574625\_mux4to1/testbench\_isim\_beh.exe" -intstyle ise -gui -tclbatch isim.cmd -wdb "C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1\_67574625\_mux4to1/testbench\_isim\_beh.wdb"

ISim simulation engine GUI launched successfully

Process "Simulate Behavioral Model" completed successfully

**6 Waveform**

Note: inputs and outputs are all 1-Bit

